Preliminary Specification

RCL Semiconductors Ltd.

8-Bit Serial-in/Parallel-out Shift Register HC164A

GENERAL DESCRIPTION

HC164A is fabricated in the high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

This 8-bit Shift Register has AND-gated serial inputs and clear. Each register bit is a D-type master-slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables

another input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only data meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive edge of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear (CL) input.

HC164A logic is functionally as well as pin-out compatible with the standard LS164. All inputs are protected from ESD damage by internal diode clamps to Vcc and ground.

FEATURES

- Wide operating supply voltage range: 2-6V.
- Asynchronous master reset $\overline{CL}$ active at low
- Date serially shifted at the positive edge of clock CK
- Low input current: $< 1\mu A$.
- Low quiescent supply current: $80\mu A$ maximum (74HC series).
- Output driving capability: standard

LOGIC DIAGRAM
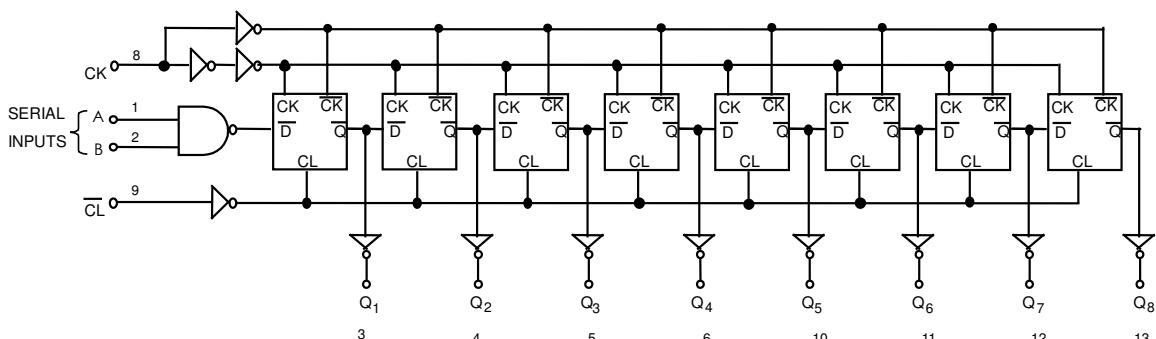
FUNCTIONAL DESCRIPTION

1. Truth Table

Inputs				Outputs			
$\overline{CL}$	CK	A	B	Q_1	Q_2	…	Q_8
L	X	X	X	L	L		L
H	L	X	X	Q_{1O}	Q_{2O}		Q_{8O}
H	↑	H	H	H	Q_{1N}		Q_{7N}
H	↑	L	X	L	Q_{1N}		Q_{7N}
H	↑	X	L	L	Q_{1N}		Q_{7N}

H = High Level (steady state). L= Low Level (steady state)

X = don't care (any input, including transitions)

↑ = Transition from low to high level.

Q_{1O} , Q_{2O} , Q_{8O} = the level of Q1 , Q2 , Q8 , respectively, before the indicated steady state input conditions were established.

Q_{1N} , Q_{7N} = The level of Q1 or Q7 before the most recent ↑ transition of the clock; indicates a one-bit shift.

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2. Logic Waveform
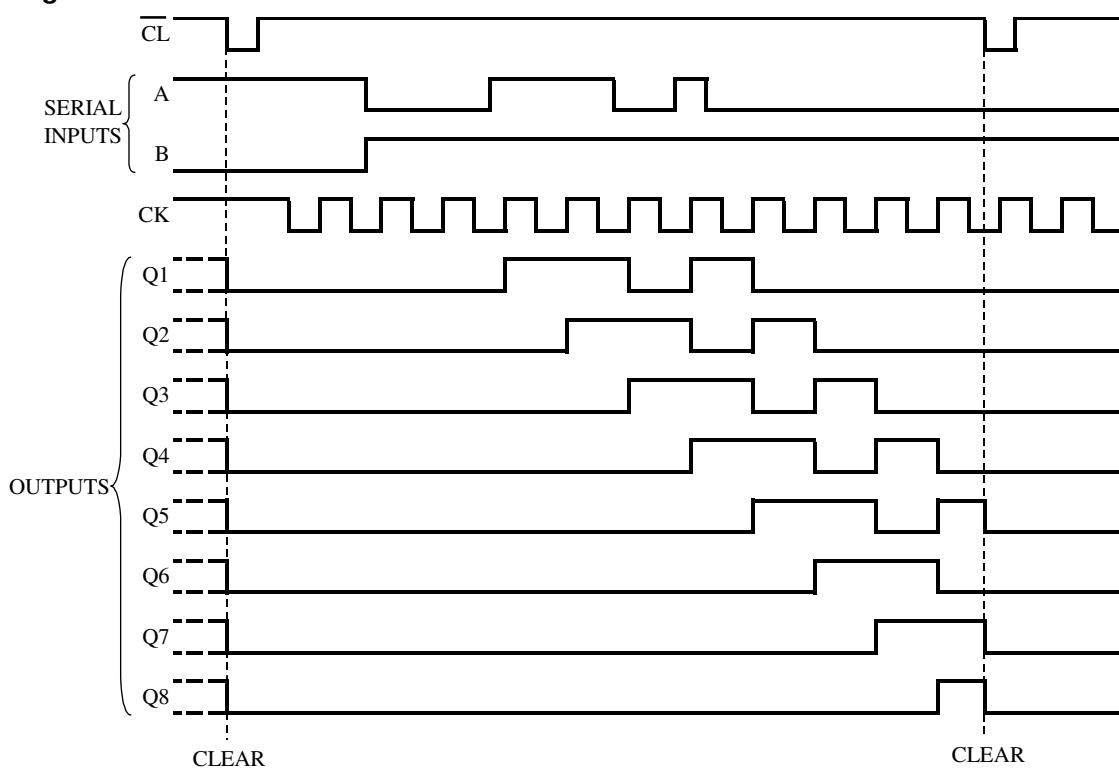
ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage (Vcc)	- 0.5 ~ + 7.0	V
DC input or output Voltage (V$_{IN}$, V$_{OUT}$)	-0.5 to Vcc +0.5	V
DC Current Drain per pin, any output (I$_{out}$)	±25	mA
DC Current Vcc or GND (Icc)	±50	mA
Storage Temperature(T$_{STG}$)	-65 ~ +150	℃
Power Dissipation (P$_D$)	500	mW

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITIONS

Parameter		Min.	Typ.	Max.	Unit
DC Supply Voltage (Vcc)		2	5	6	V
Input / output Voltage (V$_{IN}$, V$_{OUT}$)		0		Vcc	V
V$_{IH}$ High-level Input Voltage	Vcc = 2 V	1.5			V
	Vcc = 4.5 V	3.15			
	Vcc = 6 V	4.2			
V$_{IL}$ Low-level Input Voltage	Vcc = 2 V			0.5	V
	Vcc = 4.5 V			1.35	
	Vcc = 6 V			1.8	
Input Rise/Fall Times (t$_r$/t$_f$)	Vcc = 2 V			1000	ns
	Vcc = 4.5 V			500	
	Vcc = 6 V			400	
Operating Temperature (T$_A$)	74HC164A	-40		+85	℃
	54HC164A	-55		+125	℃

Note 2: All unused inputs of the device must be held at Vcc or GND to ensure proper device operation.

RCL reserves the right to make changes to this specification at any time without notice

DC ELECTRICAL CHARACTERISTICS

(apply across temperature range unless otherwise specified)

Parameter	Test Conditions		Vcc	$T_A=25^oC$ Min. Typ. Max.			54HC164A Min. Max.		74HC164A Min. Max.		Unit
V_{OH}	$V_I=V_{IH}$ or V_{IL}	I_{OH} = -20uA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		I_{OH} = -4mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -5.2mA	6V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I=V_{IH}$ or V_{IL}	I_{OH} = 20uA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6V		0.001	0.1		0.1		0.1	
		I_{OH} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OH} = 5.2mA	6V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		6V			8		160		80	μA
C_i			2V~6V		3	10		10		10	pF

TIMING REQUIREMENTS OVER RECOMMENDED OPERATING TEMPERATURE RANGE (unless otherwise noted)

Parameter			Vcc	$T_A=25^oC$ Min. Max.		54HC164A Min. Max.		74HC164A Min. Max.		Unit
f_{clock} Clock frequency			2V		6		4.2		5	MHz
			4.5V		31		21		25	
			6V		36		25		28	
t_w Pulse duration	$\overline{CL}$ low		2V	100		150		125		ns
			4.5V	20		30		25		
			6V	17		25		21		
	CK High or low		2V	80		120		100		
			4.5V	16		24		20		
			6V	14		20		18		
t_s Setup time (before CK ↑)	Data		2V	100		150		125		ns
			4.5V	20		30		25		
			6V	17		25		21		
	$\overline{CL}$ inactive		2V	100		150		125		
			4.5V	20		30		25		
			6V	17		25		21		
t_h Hold time (Data after CK ↑)			2V	5		5		5		ns
			4.5V	5		5		5		
			6V	5		5		5		

AC ELECTRICAL CHARACTERISTICS (C$_L$=50pF)

Parameter	From (Input)	To (Output)	Vcc	$T_A=25^oC$ Min.	Typ.	Max.	54HC164A Min.	Max.	74HC164A Min.	Max.	Unit
f_{max}			2V	6	10		4.2		5		MHz
			4.5V	31	54		21		25		
			6V	36	62		25		28		
t_{PHL}	$\overline{CL}$	Any Q	2V		140	205		295		255	ns
			4.5V		28	41		59		51	
			6V		24	35		51		46	
t_{pd}	CK	Any Q	2V		115	175		265		220	ns
			4.5V		23	35		53		44	
			6V		20	30		45		38	
t_t			2V		38	75		110		95	ns
			4.5V		8	15		22		19	
			6V		6	13		19		16	

Parameter	Test Conductions	Typ.	Unit
C_{pd} Power Dissipation Capacitance	$T_A=25^oC$, NO LOAD	135	pF

Note 3 : C_{PD} determines the no load dynamic power consumption , $P_D=C_{PD}*Vcc^2*f_i+ Icc*Vcc$, and the no load dynamic current consumption, $Is = C_{PD}*Vcc*f_i + Icc$.

## AC SWITCHING WAVEFORM AND AC TEST CIRCUIT
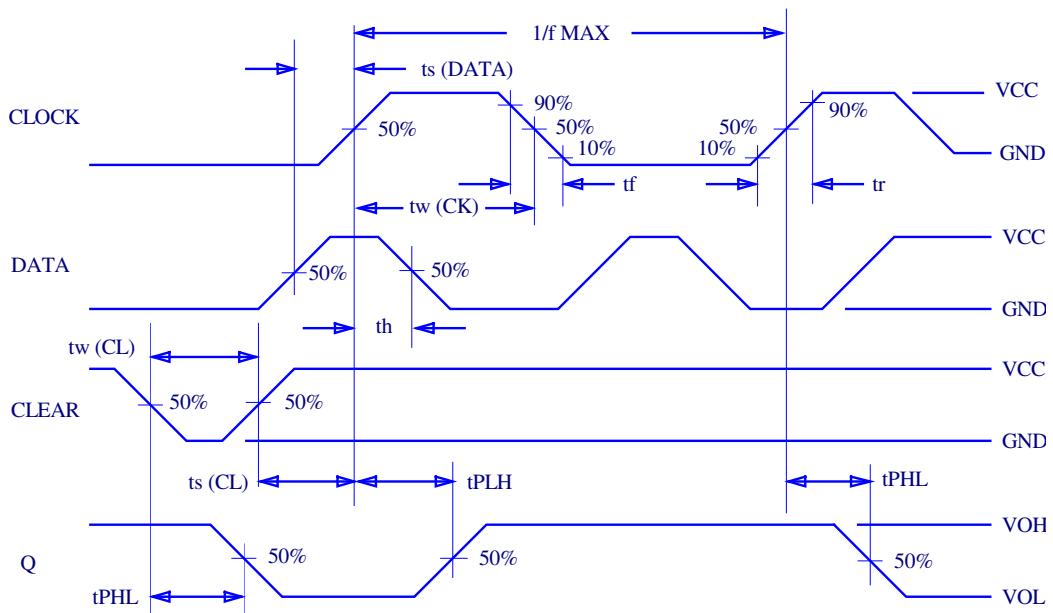
AC Switching Waveform
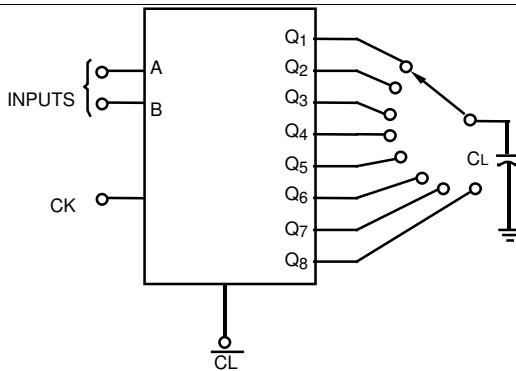
AC Testing Circuit

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	$Q_1 - Q_8$	Outputs
7	GND	Ground (0V)
8	CK	Clock input (active at rising edge)
9	$\overline{CL}$	Master reset input (active at Low)
14	V_{CC}	Positive power supply
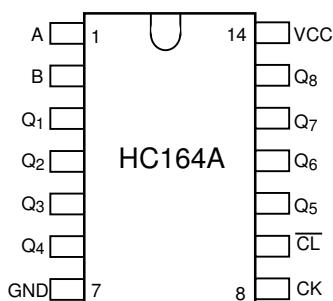
Pin Configuration (DIP14)
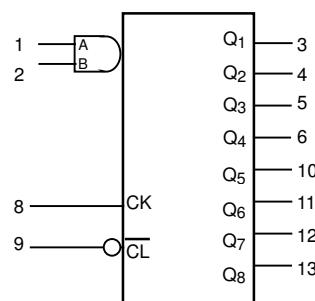
Logic Symbol

PAD DIAGRAM
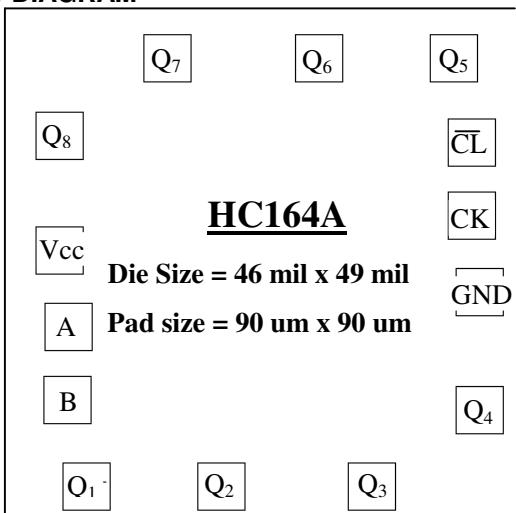
The Coordinate of Each Pad

Q_1 (-395.1, -452.8)		Q_5 (305.0, 362.8)
Q_2 (-138.3, -452.8)		Q_6 (48.2, 362.8)
Q_3 (149.9, -452.8)		Q_7 (-240.0, 362.8)
Q_4 (355.4, -308.2)		Q_8 (-445.5, 214.6)
GND (355.4, - 82.2)		Vcc (-445.5, - 3.8)
CK (338.7, 61.8)		A (-428.8, -148.8)
$\overline{CL}$ (340.6, 201.8)		B (-430.7, -288.8)

Note 4: Substrate should be connected to Vcc or left it open.